

# Computer Simulations and Experimental Investigation of the Heterodyne Employing Printed Circuit Board With an Increased Resistance to Electrostatic Discharges

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**Abstract**—We have performed computer simulations and experimental studies of characteristics of a standard analog device—the heterodyne employing a printed circuit board (PCB) made from a composite dielectric with a controlled dark conductivity. Simulation results show that an increased conductivity of the PCB smaller than  $2 \times 10^{-7} \Omega^{-1} \cdot \text{m}^{-1}$  has almost no effect on the operating characteristics of a heterodyne operating in the frequency range of 9–37 MHz, which are in a good agreement with the experimental data. Such PCBs are expected to exclude electrostatic discharges in spacecraft electronic devices otherwise occurring in them due to their internal charging by the ambient space plasma.

**Index Terms**—Charging and electrostatic discharges (ESDs), composite dielectric, computer simulation, conductivity, heterodyne, printed circuit board (PCB), radio engineering devices.

## I. INTRODUCTION

SPACECRAFT functioning on the Earth orbit is in contact with the space plasma and is bombarded by the incident electrons. As a result, spacecraft insulating materials begin to accumulate space charges. If material bulk conductivity is about  $10^{-15} \Omega^{-1} \cdot \text{m}^{-1}$ , the spacecraft surface potentials rise and the potential differences between different parts of the spacecraft gradually increase, leading frequently to the initiation of electrostatic discharges (ESDs) [1], [2]. Currents and pick-up voltages appear at the inputs of electronic devices causing their malfunctions or even complete failures [3]. As a rule, this occurs during magnetic substorms in the Earth magnetosphere.

CRRES data show that internal charging of the spacecraft electronics is especially dangerous for equipment operation [4]. However, developing effective protection against these factors is expected and is a complex engineering problem. Direct method to exclude ESD on board spacecraft

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consists in employing composite dielectrics with an increased dark conductivity [5]. These may be prepared by adding in a controlled manner a fine carbon black or a metal powder into the dielectric. It has been found that bulk conductivity of approximately  $10^{-10} \Omega^{-1} \cdot \text{m}^{-1}$  suffices to exclude ESD in spacecraft printed circuit boards (PCBs).

Eliminating ESDs is an important first step in developing the protection strategy against an internal spacecraft charging. The second one should ensure that an increased conductivity of a composite dielectric would not affect the operation of the spacecraft electronics.

Our previous work with a typical prototype of the digital electronics the low-frequency multivibrator has demonstrated that there are no changes in its operating characteristics for a bulk conductivity not exceeding  $1.5 \times 10^{-10} \Omega^{-1} \cdot \text{m}^{-1}$ , thus implying their application in PCBs for spacecraft protection against internal charging hazardous effects [6]. However, designers and technologists of electronic equipment still resist developing or employing such dielectrics even for PCBs.

This paper extends this approach to yet another class of electronics, namely, analog radio devices operating on high frequencies and short waves (e.g., heterodyne). Also, we aim to give recommendations for spacecraft engineers on how to employ poor dielectrics in PCBs. It has been shown that such an approach allows eliminating ESDs even in the worst case charging scenario without degradation of the operation characteristics of the spacecraft electronics.

## II. THEORETICAL PART

For numerical simulations, we selected the heterodyne operating in the frequency range of 9–37 MHz and generating sine wave oscillations Fig. 1(a). Fig. 1(b) shows the waveform of the output voltage at a frequency of 18 MHz.

Generally, this frequency can be estimated by the following formula:

$$f = \frac{1}{2\pi \sqrt{L_1 \frac{C_2 C_3}{C_2 + C_3}}}$$

Simulations have been done for three frequencies: 9, 18, and 37 MHz. Values of inductors  $L_1$ , capacitors  $C_2$  and  $C_3$  in Fig. 1(b) are presented in Table I.

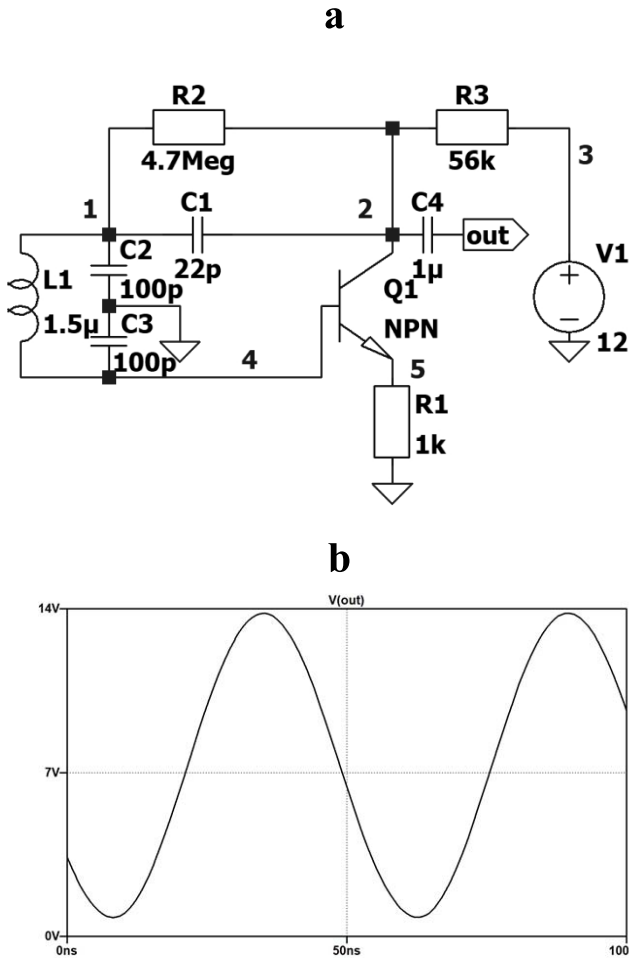


Fig. 1. (a) Computer model of the heterodyne. (b) Waveform of the output voltage (frequency 18 MHz).

TABLE I

$L_1$ ,  $C_2$ , AND  $C_3$  VALUES IN COMPUTER HETERODYNE MODEL FOR DIFFERENT FREQUENCIES

Frequency	$L_1$	$C_2$	$C_3$
9 MHz	6 $\mu$ H	100 pF	100 pF
18 MHz	1.5 $\mu$ H	100 pF	100 pF
37 MHz	1.5 $\mu$ H	25 pF	25 pF

The main operating characteristics of a heterodyne are the carrier frequency and the amplitude of the output voltage. We were looking for the upper boundary of the bulk conductivity still not affecting device characteristics, which is equivalent to introducing leakage channels between circuit junctions or to the ground.

It is usual to treat standard dielectrics as an infinite resistance between circuit junctions. In our case, these leakage resistors should be ascribed the specified finite values.

In this paper, the PCB is considered as the plane-parallel two-sided capacitor. Its resistance  $R$  and capacitance  $C$  are related by the following expression:

$$R = \frac{\epsilon_0 \cdot \epsilon}{\gamma \cdot C} \tag{1}$$

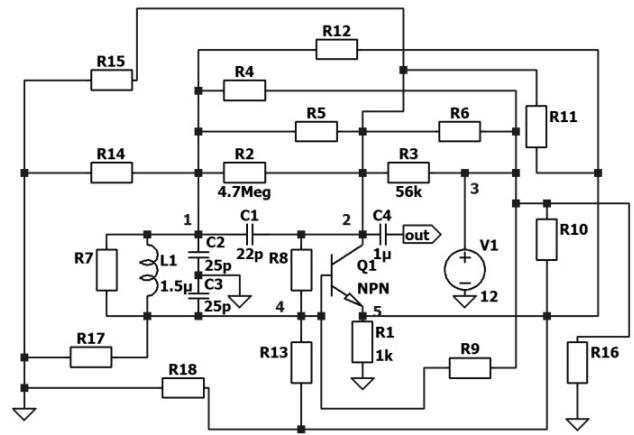


Fig. 2. Computer model of a heterodyne containing leakage channels between PCB circuit junctions.

where  $\gamma$  is the dark conductivity of a dielectric;  $\epsilon_0 = 8.85 \cdot 10^{-12} \text{ F} \cdot \text{m}^{-1}$  is the electrical constant, and  $\epsilon$  is the relative dielectric constant of a dielectric.

PCB capacitance depends on its design but the worst case implies its high value which is of prime interest to us. For mechanical reasons, two-sided PCBs for spacecraft application are usually restricted to a thickness of about 1.5 mm [7], [8].

Intrinsic capacitance of the printed board is given by

$$C = \frac{0.00885\epsilon S}{d} \text{ pF} \tag{2}$$

where  $S$  is the area of conductors (in  $\text{mm}^2$ ) and  $d$  is the printed board thickness (in mm). Stray capacitances between conductors should also be taken into account though these are sought to be minimized. For a conductor gap of 1.3 mm, they constitute 0.1–2 pF. Formula (2) allows to assess the capacitance between opposite conductors for a glass fiber board ( $\epsilon = 4.7$ ,  $d = 1.5 \text{ mm}$ ) as 3 pF/cm<sup>2</sup> [9]. We are interested in the highest value of this quantity. Formula (2) also shows that the higher is the board capacitance the lower is its resistance.

The conductor width, as a rule, does not exceed 1 mm while conductor spacing is usually two times larger. Distances between signal conductors and shielding planes in multilayer boards are a fraction of a millimeter. Such PCBs have smaller capacitances.

Taking into account that an elimination of ESDs requires a specific conductivity of  $10^{-10} \Omega^{-1} \cdot \text{m}^{-1}$  [9] and using expressions (1) and (2), we estimated the capacitances of multilateral printed boards to be in the range of 5–20 pF, while computer simulations have been conducted for leakage resistances of 3–200 M $\Omega$ .

There are two circuit methods to account for current leakages with the controlled increased conductivity. These are as follows.

- 1) Adding a number of resistances imitating leakage channels between all nodes with due account for the topology of its conductors (Fig. 2). Also, we assume resistors R4–R18 imitating leakage channels to be equal depending on a specific value of the enhanced conductivity.

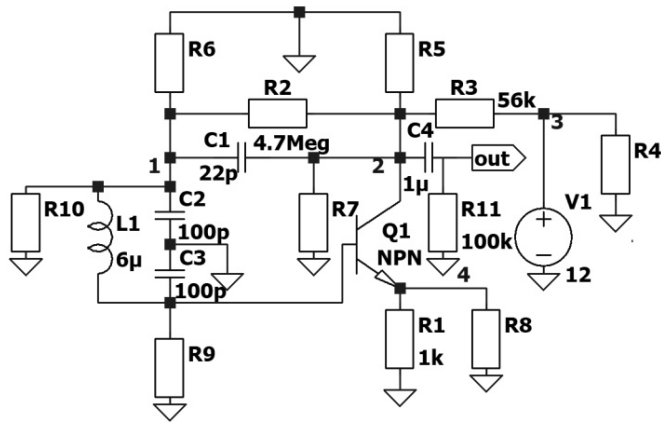


Fig. 3. Computer model of a heterodyne equipped with leakage channels to the ground.

TABLE II

SIMULATION RESULTS OF A HETERODYNE USING THE FIRST METHOD

		$\infty$	200 M $\Omega$	50 M $\Omega$	20 M $\Omega$	10 M $\Omega$	3 M $\Omega$
37 MHz	T, ns	27,3	27,2	27,1	27,3	27,2	26,8
	f, MHz	36,9	36,8	36,9	36,6	36,7	37,3
	V <sub>outs</sub> , V	6.74	6.73	6.63	6.42	6.13	5.01
18 MHz	T, ns	54,4	54,1	54,2	54,4	54,1	54,7
	f, MHz	18,4	18,5	18,4	18,4	18,5	18,3
	V <sub>outs</sub> , V	6.83	6.85	6.75	6.17	5,9	4,81
9 MHz	T, ns	108,3	108,3	108,3	108,3	108,3	108,7
	f, MHz	9,23	9,24	9,24	9,23	9,23	9,2
	V <sub>outs</sub> , V	6.75	6,8	6,75	6,75	6,55	5,14

2) The same is true for the case of leakage channels connecting conductors to the ground (Fig. 3). Again, resistors R4–R11 have identical values.

In reality, resistors R4–R18 may differ markedly. Considering that the range of investigated leakage resistances grossly overlaps these differences roughly by two orders of magnitude (from 3 to 200 M $\Omega$ ), these may be assumed equal indeed. As a result, it becomes possible to associate heterodyne changes in response to added leakage resistors with specific PCB conductivity. The latter may be taken as a criterion for developing the discharge-free spacecraft electronics.

### III. MODELING

Heterodyne simulation results for three frequencies 9, 18, and 37 MHz and a set of leakage resistances are presented in Table II.

Table II uses the following designations: T - voltage signal period, f - its frequency, and V<sub>amp</sub> - its amplitude;  $\infty$  - heterodyne characteristics without leakage resistances, while 200 M $\Omega$  denotes the value of leakage resistors.

According to Fig. 4, frequency changes of a signal that would exceed a simulation error were not observed. As demonstrated in Table II, the amplitude of the voltage output begins

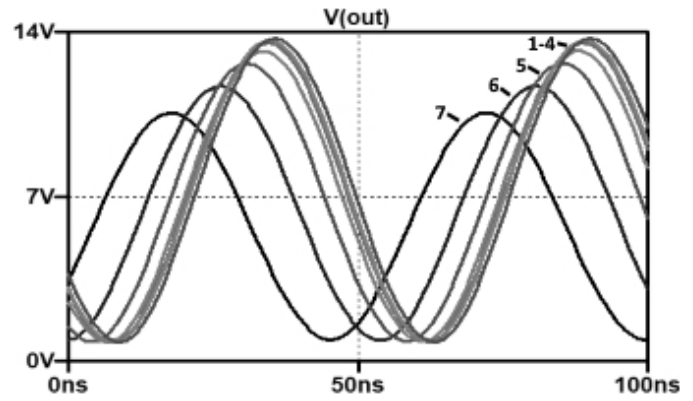


Fig. 4. Voltage signals predicted by a heterodyne simulation using the first method. Resistance values: 1–4–200, 100, 50, and 20 M $\Omega$ , respectively; 5–10 M $\Omega$ ; 6–5 M $\Omega$ ; and 7–3 M $\Omega$ .

TABLE III

SIMULATION RESULTS OF THE HETERODYNE VOLTAGE AMPLITUDE BY THE SECOND METHOD

		$\infty$	200 M $\Omega$	100 M $\Omega$	50 M $\Omega$	10 M $\Omega$	3 M $\Omega$
37 MHz	V <sub>outs</sub> , V	6.7	6.7	6.7	6.7	6.6	6.2
18 MHz	V <sub>outs</sub> , V	5.7	5.7	5.7	5.7	5.7	5.4
9 MHz	V <sub>outs</sub> , V	6.0	6.0	6.0	6.0	6.0	5.7

to decrease noticeably for small leakage resistances. From Fig. 5(a)–(c), it follows that the voltage amplitude drops considerably as leakage resistance drops from 200 to 3 M $\Omega$  for all operating frequencies.

The voltage amplitude falls from 6.74 to 6.13 V for a leakage resistance change from 200 to 20 M $\Omega$  which corresponds to a 9% decrease of the voltage amplitude irrespective of frequency. Noticeable influence begins only if resistance falls from 20 to 3 M $\Omega$ . At 9 MHz, a noticeable influence begins from 5 M $\Omega$  downward (Fig. 5).

Results of computer simulations by the second method are given in Table III and Fig. 6. Observable changes in the voltage amplitude begin from 3 M $\Omega$  downward.

Simulation results show that heterodyne characteristics are more susceptible to the interconductor leakage resistances rather than grounding ones. As a result, we define the leakage resistance 20 M $\Omega$  as a universal minimum value still guaranteeing an undisturbed heterodyne operation at all frequencies studied.

Both methods show that functional characteristics of a heterodyne (frequency and output amplitude) begin to change when resistances defining these characteristics (e.g., R2 in Figs. 2 and 3) become comparable with that of respective leakage channels.

Now, we calculate the bulk conductivity of the PCB with a minimum leakage resistance 20 M $\Omega$ . With the standard width of the printing conductor as 0.5 mm and the distance between the conductor and the screen as 1.5 mm for PCBs with a

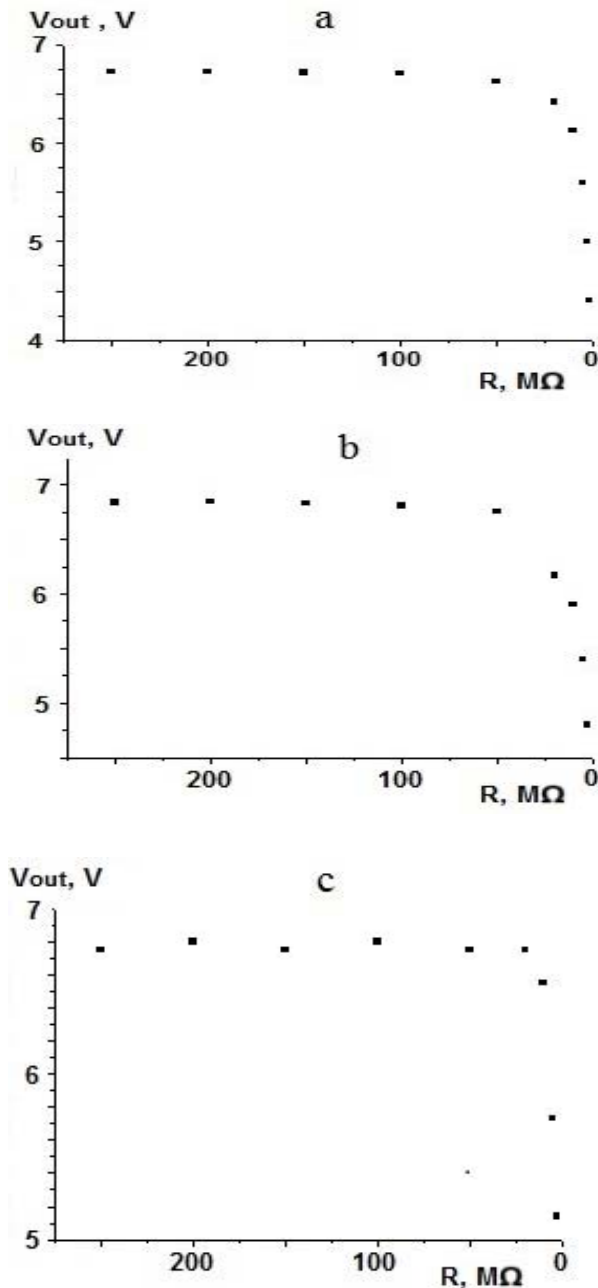


Fig. 5. Voltage amplitudes of a heterodyne as a function of resistance used. Operating frequency. (a) 37 MHz. (b) 18 MHz. (c) 9 MHz.

shielding plane, we evaluate the stray capacitance as 8 pF. The relative dielectric constant of the composite insulator was taken to be  $\epsilon = 3.5$ .

Then, according to formula (1), we find the sought conductivity value

$$\gamma = \frac{\epsilon \cdot \epsilon}{R \cdot C} = \frac{8.85 \cdot 10^{-12} \cdot 3.5}{20 \cdot 10^6 \cdot 8 \cdot 10^{-12}} = 1.95 \cdot 10^{-7} \Omega^{-1} \cdot \text{m}^{-1}$$

Therefore, to keep characteristics of a heterodyne within specifications and exclude ESDs, it is recommended to use composite dielectrics with specific bulk conductivity  $2 \times 10^{-7} \Omega^{-1} \cdot \text{m}^{-1}$ . It is two orders of magnitude larger than the critical conductivity  $10^{-10} \Omega^{-1} \cdot \text{m}^{-1}$  excluding ESDs.

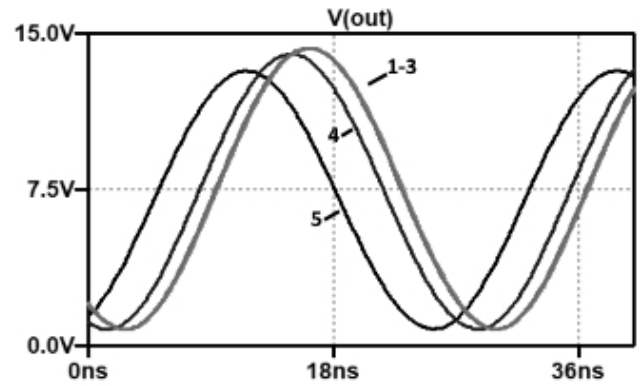


Fig. 6. Voltage signals predicted by a heterodyne simulation using the first method. Resistance values: 1-3-200, 100, and 50 MΩ; 4-10 MΩ; and 5-3 MΩ.

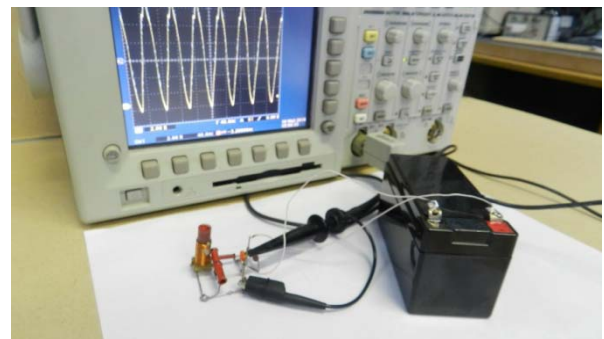


Fig. 7. Prototype of a heterodyne with the PCB dielectric made from a composite material with an enhanced conductivity shown together with the measuring unit.

#### IV. EXPERIMENTAL VALIDATION

To test simulation results, we fabricated a prototype heterodyne based on the electric circuit shown in Fig. 1, as explicitly described in [5].

This heterodyne with soldered wires to supply voltage and transmit an output signal was put in a Petri dish and warmed up to 60 °C in a heat oven. Then, the molten composite material was poured into the dish. The composite consisted of paraffin mixed with 9.1% mass of the technical carbon with bulk conductivity of  $5 \times 10^{-9} \Omega^{-1} \cdot \text{m}^{-1}$ . According to [5] and [6], it should prevent ESDs.

After cooling this assembly to the ambient temperature, we checked heterodyne operation. Measurements were made at a reference frequency of 18 MHz. To register the output signal, we used a digital oscilloscope Tektronix 3012B (Fig. 7).

We compared experimental data for a heterodyne using a printed board with an enhanced conductivity with analogous simulation data for leakage resistors 200 MΩ (Fig. 8). For conductivity value  $5 \cdot 10^{-9} \Omega^{-1} \cdot \text{m}^{-1}$ , leakage resistance according to formula (1) is much higher than the maximum simulated value of 200 MΩ which has no effect on the heterodyne output characteristics.

It is seen that the frequency and amplitude of the voltage output (17.2 MHz and 6.45 V) for the prototype heterodyne slightly differ from those obtained in simulations (18.5 MHz and 6.85 V). These differences are 7% and 5.8%, respectively,

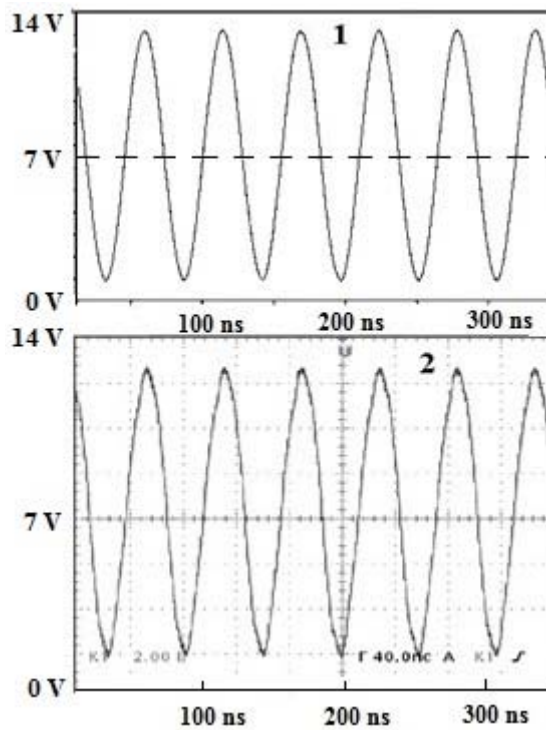


Fig. 8. Diagrams of the voltage output of a heterodyne. 1—as given by the simulation for the leakage resistance of 200 MΩ. 2—experimental results.

and are due to simulation errors because, in simulations, real values of resistors, capacitors, and inductors were not used.

According to expression (1), the resistance of 200 MΩ corresponds to the bulk conductivity of the composite material approximately equal to  $5 \cdot 10^{-9} \Omega^{-1} \cdot \text{m}^{-1}$  when the capacitance of the PCB is  $C = 20 \text{ pF}$ .

Thus, experiments on a prototype heterodyne using the composite dielectric with an increased conductivity have fully validated simulation results. Accordingly, such composite dielectrics provide an adequate draining path for the space charge implanted by space plasma electrons, without thus excluding any degradation of spacecraft electronics. So, we consider that such an approach may be effective in qualifying PCBs for spacecraft application.

### V. CONCLUSION

Computer simulations and experimental studies have been carried out to investigate characteristics of a typical analog

device the heterodyne employing PCBs with substituted insulators made from composite dielectrics having an increased and controlled dark conductivity. Simulation results show that increase in conductivity of the PCB material up to  $2 \times 10^{-7} \Omega^{-1} \cdot \text{m}^{-1}$  has practically no effect on heterodyne characteristics in the frequency range of 9–37 MHz in full accord with experimental data. It has been shown that the proposed approach may prove helpful for the development of space qualified discharge-free electronic devices.

We define the PCB conductivity range which does not interfere with an operation of the spacecraft electronics. Guidelines for creating ESD-free spacecraft have been formulated which can be further extended using existing printed board design codes providing calculations of the stray capacitances between board conductors. This, in turn, allows assessing the values of extra resistors using (1). In the future, we plan to demonstrate the feasibility of substituting all spacecraft dielectrics with those having an enhanced conductivity, thus substantially mitigating the spacecraft charging problems.

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### REFERENCES

- [1] Henry B. Garrett, Albert C. Whittlesey, *Guide to Mitigating Spacecraft Charging Effects*. 1st ed. Hoboken, NJ, USA: Wiley, 2012.
- [2] D.C. Ferguson, “Low earth orbit spacecraft charging design handbook,” NASA, Washington, DC, USA, Tech. Rep. NASAHDBK-4006, Jun. 2007.
- [3] J. P. Catani and D. Payan, “Electrostatic behaviour of materials in a charging space environment,” in *Proc. IEEE Int. Conf. Solid Dielectr.*, Jul. 2004, pp. 917–927.
- [4] A. R. Frederickson, “Upsets related to spacecraft charging,” *IEEE Trans. Nucl. Sci.*, vol. 43, no. 2, pp. 426–441, Apr. 1996.
- [5] V. S. Saenko, A. P. Tyutnev, A. E. Abrameshin, and G. A. Belik, “Computer simulations and experimental verification of the nanoconductivity concept for the spacecraft electronics,” *IEEE Trans. Plasma Sci.*, vol. 45, no. 8, pp. 1843–1846, Aug. 2017.
- [6] E. D. Pozhidaev, V. S. Saenko, and A. E. Abrameshin, “Simulation and the experimental study of characteristics of the radio engineering nodes executed on PCB with the increased resistance to ESD (in Russian),” *Tekhnologii Ehlektromagnitnoj Sovmestivosti Technol. Elektromagn. Compat.*, vol. 56, no. 1, pp. 34–40g, 2016.
- [7] J. L. Sloan, *Design and Packaging of Electronic Equipment*. New York, NY, USA: Van Nostrand Reinhold Company Inc., 1985.
- [8] C. K. Purvis, H. B. Garrett, A. C. Whittlesey, and N. J. Stevens, “Design guidelines for assessing and controlling spacecraft charging effects,” NASA, Washington, DC, USA, Tech. Rep. 2361, Sep. 1984.
- [9] (2018). *Printed Circuit Board (PCB) Design Issues*. [Online]. Available: <https://www.analog.com/media/en/training-seminars/design-handbooks/Basic-Linear-Design/Chapter12.pdf>